A Sub-\(\mu\)W Bandgap Reference Circuit With an Inherent Curvature-Compensation Property

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Abstract—A new current-mode bandgap reference circuit (BGR) which is capable of generating sub-1-V output voltage is presented. It has not only the lowest theoretical minimum current consumption among published current-mode BGRs, but also additional advantages of an inherent curvature-compensation function and not requiring NPN BJTs. The curvature-compensation is achieved by utilizing the exponential behavior of sub-threshold CMOS transistors to compensate the BJT base-emitter voltage high-order temperature dependence. By taking advantages of the continuing development of CMOS technology, sub-\(\mu\)W power consumption is achieved with a reasonable core area. Related design considerations and challenges are discussed and analyzed. The proposed BGR is realized in a TSMC 90 nm process. Measurement results show a temperature coefficient without trimming as low as 10.1 ppm/°C over a temperature range of 70 °C because of the proposed curvature-compensation technique. The average value is 32.6 ppm/°C which could be improved by trimming resistor ratios. The average power consumption at room temperature is 576 nW, with a core area of only 0.028 mm\(^2\).

Index Terms—bandgap reference, CMOS, curvature-compensation, low-power, nano-meter (nm), nano-watt (nW), wireless sensor network.

I. INTRODUCTION

BANDGAP reference circuits (BGR) generate precise reference signals which are insensitive to process, voltage and temperature variations and have been used for decades because of their reliability. One of the major BGR design parameters is temperature coefficient (TC). For CMOS BGRs, this non-ideality is mainly due to the high-order temperature dependence of BJT base-emitter voltage \(V_{BE}\). Different curvature-compensation techniques have been developed, for example [1]–[9] etc. In [1] and [2], a non-linear current, which is generated by using an extra BJT, is applied to compensate the high-order temperature dependence. Piecewise-linear curvature-compensation technique has been proposed in [3] and adopted in [4]–[7], a CMOS non-linear current source is turned on and added to the output when the operating temperature is higher than a pre-determined value. As a result, the second-order behavior is corrected and the TC performance is improved by extending the temperature range. In [8], two current-mode BGRs, one of them using PNP BJTs and the other one using NPN BJTs, are constructed. Because they have similar temperature dependence, a second-order curvature-compensation can be achieved by subtracting their output current with a proper scale. Most curvature-compensation techniques require additional components and power consumption. A remarkable exception is [9], the BGR high-order temperature dependence is compensated by incorporating two different types of resistor whose first-order TCs are of opposite sign. Nevertheless intensive trimming may be needed to match the resistor ratios because the resistors are with different types. More curvature-compensation techniques and related discussion can be found in [10].

Another consideration is the power consumption. Sub-\(\mu\)W, or even lower, power consumption is targeted for power-aware applications such as medical devices and wireless sensor networks [11]–[14]. However only a few sub-\(\mu\)W BGRs can be found in literature [13]–[16]. This is because most BGRs contain resistors for voltage-to-current (V-to-I) conversion and/or vice versa, large resistance is needed in order to achieve such power consumption level. This can increase the chip area substantially. As a result, some research [17]–[19] has been conducted on non-bandgap CMOS-only reference circuits which generate the output voltage based on MOS transistor threshold voltage \(V_{TH}\). The trade-off is a relatively large output error due to process variations [17], for example a coefficient of variation of 4% is measured in [18] which is worse than that for BGRs (around 1% in [14] and [20]). This is because the \(V_{TH}\) variation over process corners can be as large as ±15%, while the bandgap voltage variation is usually within ±1%. Trimming could be used to improve this error, but is undesirable due to increased area, cost and testing time.

The minimum width of resistors scales down with the continuing aggressive development of CMOS technology. Mega-ohm resistors can be realized with a reasonable area in state-of-the-art CMOS processes, hence sub-\(\mu\)W BGR power consumption is now achievable. For example the high-resistance poly resistor without salicide in the 90 nm CMOS process used in this work, its resistivity can be as large as 0.16 MΩ per 100 \(\mu\)m\(^2\) and would increase even more favorably with more modern technology nodes. The drawbacks are the need of an extra salicide-blocking mask and, hence, increased fabrication cost. The resistor area is now less dominating, and becomes comparable to other components for BGR design.

In this work, a new current-mode BGR topology with an inherent curvature-compensation property is proposed. By taking advantages of technology scaling, high-precision, low-power and small-area BGRs become flexible in modern nm CMOS technology. While MOS transistors do not benefit much in analog circuit design from the scaling, non-idealities such as short channel effects and gate leakage become even more...
problematic. BGR design in nm CMOS technology is studied. A proof-of-concept prototype is realized in a TSMC 90 nm CMOS process and shows good results.

This paper is organized as follows. Challenges and design issues of implementing BGRs in modern nm CMOS processes are discussed in Section II. Section III analyzes the proposed BGR and curvature-compensation technique. Verifications of the proposed BGR and discussion are presented in Section IV. Section V concludes the paper.

II. BGR DESIGN IN NM CMOS PROCESSES

A. Basic BGR Topologies

Fig. 1 shows a widely-used BGR structure. It can be shown that

\[ V_O = V_{EB1} + n \ln(N) \frac{R_2}{R_1} \cdot V_T \]

where \( n \) is the diode non-ideal factor, \( N \) is the ratio between Q1 and Q2, \( V_T \) is the thermal voltage, \( k \) is the Boltzmann constant, \( T \) is the absolute temperature, and \( q \) is the elementary charge of an electron. \( V_T \) is a proportional-to-absolute-temperature (PTAT) parameter with TC of approximately 85 \( \mu \text{V/}^\circ\text{C} \), on the contrary \( V_{BE} \) (or \( V_{BE} \) for NPN BJTs) is a complementary-to-absolute-temperature (CTAT) parameter with TC of approximately -1.6 \( \text{mV/}^\circ\text{C} \) [21]. If we ignore high-order effects, \( V_O \) can be set to be first-order temperature-independent by sizing \( N \) and the ratio between \( R_1 \) and \( R_2 \) such that

\[ M = n \ln(N) \frac{R_2}{R_1} = \frac{\Delta V_T}{\Delta T} = \frac{-1.6 \text{mV/}^\circ\text{C}}{85 \text{mV/}^\circ\text{C}} \approx 19 \]

The output voltage is fixed to be approximately 1.2 V due to the silicon bandgap voltage, this limits the usability of this BGR in modern nm CMOS processes which are targeted to operate at low supply voltage.

To achieve sub-1-V output voltage, current-mode BGRs can be used [1]–[8], [13], [22]. Most of them are based on the structure proposed by Banba et al. [22]. The schematic is shown in Fig. 2. The idea is to convert both \( V_{EB} \) and \( V_T \) into current form and sum them with a proper scale. \( V_O \) is then given as

\[ V_O = \frac{R_4}{R_2} V_{EB1} + n \ln(N) \frac{R_2}{R_1} V_T \]

The drawbacks are the additional components required and larger resistance for the V-to-I conversions. Current-mode BGRs also have the benefits of generating temperature insensitive reference current and multiple reference voltage (by replacing the output resistor with voltage dividers with the same total resistance) which may be required for large system designs [13].

One interesting variant is proposed in [5] and [13], the PTAT and CTAT current are generated independently. By scaling and summing them properly, reference current with desired TC can be generated and applied to design temperature-compensated circuits and temperature sensors [13].

B. Uses of NPN BJTs

In deep sub-\( \mu \text{m} \) CMOS processes, deep N-well layer is normally available. This enables the design of vertical NPN BJTs with moderate current gain (\( \beta > 4 \)). Note that \( \beta \) is a PTAT parameter and can vary for 30% due to process variations, the design may be more complicated if \( \beta \) is not large enough to ignore its effect. Some examples of CMOS BGRs using NPN BJTs can be found in [6] and [13]. However, unlike the BGRs shown in Fig. 1 and 2, the collector inputs of the NPN BJTs are not connected together in those structures, which potentially requires more area. Furthermore, because of the thickness of the deep N-well, the minimum size and spacing of NPN BJTs are usually larger than those of PNP BJTs for the same emitter area [15].

C. Line Sensitivity

Line sensitivity is a very important BGR design parameter, it measures the sensitivity of the output voltage (or current) to the supply voltage and indicates the low-frequency power supply rejection ratio (PSRR). It is mainly limited by the finite output resistance of current mirrors, hence very long transistors [18] or advanced current mirror structures [19], [20] are required for high-performance reference circuits. The situation is even worse in nm CMOS processes because of the halo implant, which is commonly introduced in modern CMOS technology to reduce drain-induced barrier lowering effect for short channel length CMOS transistors. However it causes a severe degradation of the output resistance for longer channel lengths [23].

Regarding the current mirror structures, normal cascade, regulated cascode [20] and gain-boosted [5], [22] topologies are widely used. The first two structures increase the headroom overhead and the latter one can only be applied to current mirrors with two branches.

D. Process Variations

One very important feature of the BGRs shown in Fig. 1 and 2 is that, to the first order, their output voltage relies only on relative size ratios between components (resistors and BJTs), but not their absolute values. Hence very good matching (mismatch can be as small as 0.1%) can be achieved by careful layout and the size constraints are reduced significantly.
However, (1) and (3) do not account for the transistor mismatch of the current mirrors. The current mismatch for transistors in strong inversion is usually modeled as [24]

\[ \sigma_{\text{IDS}} = \left( \frac{g_m}{I_D} \right)^2 \frac{A_{V_{TH}}}{W/L} + \frac{A_K}{W/L} \]  

where \( A_{V_{TH}} \) and \( A_K \) are the proportionality constants of the threshold voltage and mobility respectively, \( W \) and \( L \) are the transistor width and length respectively.\(^1\) The first term is usually dominating. Small \( g_m/I_D \) (i.e. large overdrive voltage) is preferred, but it is difficult in nm CMOS design due to the limited headroom. Large transistors would be used instead, with a trade-off of poor high-frequency PSRR due to large parasitic capacitance. Moreover, this may cause gate leakage depending on the gate oxide thickness \( t_{ox} \). We do not see significant gate leakage effect in the 90 nm CMOS process used in this work. However it has been reported in [26] that if \( t_{ox} \leq 1.7 \) nm, the gate leakage current density can be larger than 1 mA/cm\(^2\) even with small gate-source voltage \( < 250 \) mV. There may exist a trade-off between the gate leakage and transistor matching for such processes.

III. PROPOSED BANDGAP REFERENCE CIRCUIT

In this section, the proposed BGR and curvature-compensation technique are verified. So far, we assume the CTAT source \( V_{EB} \) is only first-order temperature-dependent which is not true in reality. Including the higher-order effect, \( V_{EB} \) can be written as [5], [27]

\[ V_{EB}(T) = V_{BG}(T_R) \frac{T}{T_R} [V_{EB}(T_R) - V_{BG}(T_R)] + \eta \ln \frac{T_R}{T} \]  

where \( V_{BG} \) is the bandgap voltage of silicon extrapolated to 0 K, \( T_R \) is the reference temperature, \( \eta \) is a temperature constant depends on the technology with the most representative value 3.54, and \( \zeta \) is the order of temperature dependence of collector current. The higher-order temperature dependence limits TC of first-order BGRs to be around 15 °C over a temperature range of 70 °C (see Appendix I), curvature-compensation is required in order to achieve a better TC.

The basic concept of the proposed curvature compensation-technique is to generate a nonlinear voltage \( V_{NL} \) with high-order temperature dependence of approximately \(-V_T(\eta - 1) \ln(T_R/T)\) by utilizing the exponential behavior of sub-threshold MOS transistors, meanwhile the high-order temperature dependence of \( V_{HE} \) is \( V_T(\eta - 1) \ln(T_R/T) \) as shown later. \( V_{NL} \) and \( V_{HE} \) are summed in current form to perform the curvature-compensation. Similar solutions have been proposed in [1] and [2], however the proposed BGR has lower circuit complexity and current consumption. The idea is shown in Fig. 3 and the following conditions are assumed to be valid:

- All the NMOS transistors operate in the sub-threshold region and are saturated \( V_{GS} \gg V_T \). Their drain current is then given by

\[ I_D \approx \mu C_{ox} V_{TH}^2 \frac{W}{L} \exp \left( \frac{V_{GS} - V_{TH}}{mV_T} \right) \]  

where \( \mu \) is the electron mobility, \( C_{ox} \) is the oxide capacitance per unit area, \( V_{GS} \) is the transistor gate-source voltage, and \( m \) is the transistor sub-threshold slope parameter.

- The PTAT current \( I_1 \) is first-order temperature-dependent and its higher-order temperature dependence can be ignored. Hence \( \zeta = 1 \) and \( I_1 \) can be written as

\[ I_1 = \frac{k \cdot n \ln(N)}{R_1 q} T \]  

- The high-order temperature dependence of the CTAT current \( I_2 \), which is generated from \( V_{EB} \), is compensated. More details of the temperature compensation will be shown later in this section. Thus \( I_2 \) is also first-order temperature-dependent.

- \( I_0 = I_1 + I_2 \) and \( I_0 \) is constant at all temperature, in other words \( \Delta I_1/\Delta T = -\Delta I_2/\Delta T \):

\[ I_1(T_R) = I_2(T_R) = \frac{k \cdot n \ln(N)}{R_1 q} T_R \]  

Hence \( I_0 \) can be expressed as

\[ I_0 = 2 \cdot I_1(T_R) = \frac{2k \cdot n \ln(N)}{R_1 q} T_R \]  

The situation is illustrated in Fig. 4. Short-channel effects of the MOS transistors and temperature-dependence of the resistors are negligible. It can be observed that

\[ V_{EB} + V_{GS} = V_{GS} + I_2 R_2 \]
Assume all NMOS transistors have the same size and $V_{TH}$, we have

$$I_2 = \frac{1}{R_2} V_{EB1} + \frac{1}{R_2} \left( \frac{V_{NL}}{m V_T \ln \frac{I_1}{I_2}} \right)$$

(11)

$$= \frac{1}{R_2} \left\{ V_{BG}(T_R) - \frac{T}{T_R} \left[ V_{EB}(T_R) - V_{BG}(T_R) \right] \right\}$$

Higher-order terms

(12)

By using Taylor series, if $x \approx 1$, $\ln(x) \approx x - 1$. This implies if both $I_1/I_2$ and $T_R/T$ are approximately equal to one within a certain range of temperature, the higher-order terms can be written as:

$$I_{2,HO} = \frac{V_T}{R_2} \left( -m \ln \frac{I_2}{I_1} + (\eta - 1) \ln \frac{T_R}{T} \right)$$

(13)

$$\approx \frac{V_T}{R_2} \left[ -m \left( I_2 - 1 \right) + (\eta - 1) \left( \frac{T_R}{T} - 1 \right) \right]$$

(14)

$$= \frac{V_T}{R_2} \left[ -m \frac{I_0 - I_1}{I_1} + (\eta - 1) \frac{T_R}{T} + 1 - \eta + m \right]$$

(15)

Substitute (7) and (9) into (15),

$$I_2 \approx \frac{1}{R_2} \left\{ V_{BG}(T_R) - \frac{T}{T_R} \left[ V_{EB}(T_R) - V_{BG}(T_R) \right] \right\}$$

(16)

Thus $V_O$ can be found as

$$V_O - R_3 (I_1 + I_2)$$

(19)

$$= \frac{R_3}{R_2} \left\{ V_{BG}(T_R) - \frac{T}{T_R} \left[ V_{EN}(T_R) - V_{BG}(T_R) \right] \right\}$$

Higher-order terms

(20)

And the first-order temperature-dependence can be cancelled out by setting $R_2/I_1$ to

$$\frac{R_2}{R_1} = \frac{q \left[ V_{EB}(T_R) - V_{BG}(T_R) \right]}{k \cdot m \ln(N) T_R}$$

(21)

and $V_O$ becomes

$$V_O = \frac{R_3}{R_2} \cdot V_{BG}(T_R)$$

(22)

The proposed curvature-compensation technique is simple and requires no additional current consumption. To the best of the authors’ knowledge, the BGR topology used in [13] and [15] has the lowest theoretical minimum current consumption among all current-mode BGRs and is given as

$$I_{min} = 3 \cdot I_{PTAT} + 2 \cdot I_{CTAT} = \frac{n \ln(N)}{R_{PTAT}} \left( 3V_T + 2 \frac{V_{FE}}{M} \right)$$

(23)

where $R_{PTAT}$ is the resistor used in the PTAT current generator (for example $R_1$ in Fig. 1, 2 and 3). The proposed BGR achieves the same figure but with an additional curvature-compensation function and without using NPN BJTs.

So far we assume the short-channel effects of the MOS transistors and temperature-dependence of the resistors are negligible, however this is not valid in reality. The transistors short-channel effects may cause mismatches between current mirror branches which induce output offsets and degrade TC performance. The temperature-dependence of $R_3$ introduces another PTAT/CTAT parameter which needs to be compensated by adjusting the TC of $I_0$. As a result, $I_0$ is not temperature independent as assumed, instead it has a similar temperature dependence (but of opposite sign) as $R_3$. The first-order TC of the high-resistance poly resistor used in this work is approximately $-0.02\%$ per degree Celsius ($200 \mu \text{ppm/°C}$).

IV. VERIFICATIONS

A. Post-Layout Simulation Results

The proposed BGR is designed in a TSMC 90 nm CMOS process and the schematic including start-up circuit is shown in Fig. 5. The supply voltage is 1.2 V. Assume a current mirror with 100 nA output, in order to achieve a line sensitivity of 0.1%/V, an output resistance of 10 GΩ ($= 1 \text{ V}/(0.1 \%\cdot 100 \text{ nA})$) is required. Advanced current mirror structures are needed to achieve such large output resistance. Normal cascode, instead of gain-boosted, PMOS current mirrors are adopted because the current mirror containing M1–M6 has more than two branches, the trade-off is larger required voltage headroom which may reduce the operating temperature range. This is because $V_{BE}$ and $V_{TH}$ become too large at low temperature. Using thick-gate transistors can enable larger supply voltage and, hence, wider operating temperature range, however such kind of transistors is usually not well-modeled and their larger $V_{TH}$ increases the required supply voltage. To further improve the line sensitivity performance, an operational transconductance amplifier (OTA) is added to make the voltage at nodes A and B to be approximately the same. A compensation capacitor $C_C$ of approximately 5 pF is added to improve the stability with a trade-off of longer start-up time. The NMOS transistors are put inside a deep N-well with their own substrate connected to their source, this improves the matching between their $V_{TH}$. All the transistors are with low-$V_{TH}$ type and operating in sub-threshold region to minimize the required voltage headroom.

Fig. 6 depicts the post-layout simulated temperature dependence of the proposed BGR at the typical design corner ($\{ \text{TDC} \}$) and the temperature dependence of an ideal first-order BGR with the theoretical minimum second-order nonlinearity modeled by using (27) ($\{ 11 \}^{\text{st, nd, th}}$). The proposed BGR achieves an excellent TC of 5.5 ppm/°C over the commercial temperature range (0 to 70 °C) and outer-performs the ideal first-order BGR because of the proposed curvature-compensation technique. The TC performance outside
this temperature range degrades due to the limited voltage headroom and the fact that the Taylor series assumption we made in Section III and the curvature-compensation do not hold anymore. The curvature-compensation effect can also be proved by comparing $\Delta V_{R2}/\Delta T$ (where $V_{R2} = I_{CT,AT}/R_2$) and $\Delta V_{EB}/\Delta T$, with the post-layout simulation results at the typical design corner shown in Fig. 7. From 0 to 70 °C, $\Delta V_{EB}/\Delta T$ drops around 4%, while $\Delta V_{R2}/\Delta T$ varies around 0.6% only. The post-layout simulated noise density without any decoupling capacitor at 100 Hz is 680 nV/√Hz.

To analyze the BGR sensitivity to process variations and mismatches, 100 runs of post-layout Monte Carlo simulations are performed and the results are shown in Fig. 8. Fig. 8(a) depicts $\Delta V_{R2}/\Delta T$ versus temperature. $\Delta V_{R2}/\Delta T$ increases at low temperature for some runs because of the limited voltage headroom. The TC performance over the commercial temperature range is shown in Fig. 8(b). 42 out of 100 runs achieve a TC of less than 15.1 ppm/°C and the minimum is 4.4 ppm/°C. The mean is 25.3 ppm/°C. The TC performance over a temperature range of 100 °C (0 to 100 °C) is shown in Fig. 8(c). The mean is 45.1 ppm/°C, the degradation is due to the reasons mentioned above. Note that the TC performance is not Gaussian distributed, hence it is not meaningful to calculate its standard deviation (SD). Fig. 8(d) depicts $V_O$ at room temperature, the mean and SD are 730 mV and 6.3 mV respectively which corresponds a coefficient of variation (CV) of 0.86%.

### B. Experimental Results

A proof-of-concept prototype is fabricated and packaged in a JLCC64 package. A chip microphoto and the BGR layout are shown in Fig. 9. The core area is 0.028 mm². Five sample chips are measured without trimming and the results are presented in Table I and Fig. 10, the mean of $V_O$ at 30 °C is 723 mV with a coefficient of variation of 1.3%. Sample II has the best overall performance. It achieves a TC of 10.1 ppm/°C over a temperature range of 70 °C (10 to 80 °C), which is lower than the theoretical minimum TC of first-order BGRs (15.1 ppm/°C) and proves the proposed curvature-compensation technique. We assume the variation to the targeted temperature range (0 to 70 °C) is due to the process data mismatch. The average TC over the whole measured temperature range (0 to 100 °C) is 53.1 ppm/°C which is still competitive to other sub-μW BGRs [14]–[16]. The average power consumption (including start-up
Fig. 8. Monte Carlo simulation results. (a) $\Delta V_{th}/\Delta T$, (b) TC (0 to 70 °C), (c) TC (0 to 100 °C), and (d) $V_D$.

Fig. 9. (Left) A chip microphoto. (Right) The BGR layout: A: Start-up circuit; B: CMOS transistors; C: OTA; D: $C_C$; E: Resistors; F: BJTs and dummies.

Fig. 10. Measured temperature dependence of all samples.

circuit) with a 1.2 V supply at room temperature is 576 nW and the worst-case is 640 nW at 100 °C.

Fig. 11. Measured and post-layout simulated PSRRs.

Fig. 11 depicts the measured and post-layout simulated PSRRs, the line sensitivity which is indicated by the measured low-frequency PSRR is approximately 0.3%V. MOS transistor output resistance is usually difficult to model precisely, this explains the 6 dB ($2\times$) difference between the measured and post-layout simulated low-frequency PSRRs. The measured PSRR decreases at high frequency because of the parasitic capacitance of the package, bondwires and PCB etc. The characteristic of $V_O$ versus supply voltage is shown in Fig. 12. The BGR starts to function properly when the supply voltage is higher than 1.15 V.

The measured start-up time with a 10 pF probe loading is approximately 270 μs. Nevertheless the output parasitic components cannot be modeled accurately, hence the start-up behavior
Table II

A Comparison Between the Designed BGR and Other Published State-of-the-Art Reference Circuits

<table>
<thead>
<tr>
<th>Technology</th>
<th>Curvature-compensated</th>
<th>This Work</th>
<th>Sub-(\mu)W BGRs</th>
<th>Curvature-compensated BGRs</th>
<th>Non-BG reference circuits</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>[14]</td>
<td>[15]</td>
<td>[2]</td>
<td>[6]</td>
</tr>
<tr>
<td>Curvature-compensated</td>
<td></td>
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<td>No</td>
<td>Yes</td>
<td>Yes</td>
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<td>Technology</td>
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<td>90 nm CMOS</td>
<td>0.13 (\mu)m</td>
<td>0.13 (\mu)m</td>
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<tr>
<td>Min. supply voltage (V)</td>
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<td>0.7</td>
<td>1.05</td>
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<td>0.9</td>
</tr>
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<td>Power consumption ((\mu)W)</td>
<td>0.58</td>
<td>0.053</td>
<td>0.32</td>
<td>0.2</td>
<td>0.39</td>
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<tr>
<td>Temp. range (°C)</td>
<td>10 to 80</td>
<td>0 to 100</td>
<td>40 to 120</td>
<td>0 to 70</td>
<td>0 to 80 to 150</td>
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<td>TC (ppm/°C)</td>
<td>Best 10.1</td>
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<td>N/A</td>
<td>47.1</td>
<td>7.5</td>
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<td>Output voltage (V)</td>
<td>0.72</td>
<td>0.55</td>
<td>N/A</td>
<td>0.34</td>
<td>0.62</td>
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<td>Line sensitivity ((%)/V)</td>
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<td>0.016*</td>
<td>0.7</td>
<td>0.021</td>
<td>0.01</td>
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<tr>
<td>Area (mm(^2))</td>
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<td>0.025</td>
<td>0.026</td>
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<td>0.1</td>
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<td>Coefficient of variation (%)</td>
<td>0.86 (simulated)</td>
<td>1.3 (measured)</td>
<td>1.05</td>
<td>N/A</td>
<td>N/A</td>
</tr>
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<td>Multiple reference signals</td>
<td>Trimming Yes</td>
<td>No</td>
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</table>

* Current reference of 90 nA output.

\(^\ast\) Estimated from the low-frequency PSRR.

The designed BGR has the lowest power consumption compared to other curvature-compensated BGRs. The BGR in [6] utilizes the piecewise-linear curvature-compensation technique to extend the operating temperature range and improve the TC performance, similar techniques and/or trimming could be applied to the proposed BGR for improved performance.

Compared to the \(V_{TH}\)-based CMOS-only reference circuits in [17] and [18], the designed BGR shows a better coefficient of variation. Although they have very small power consumption, the \(\pm 3\sigma\) output error due to process variations can be \(>18\%\) which limits their usability without trimming. A very interesting structure has been proposed in [28], it contains only two NMOS transistors with different \(V_{TH}\) and the output voltage is generated based on the \(V_{TH}\) difference. As a result, it is relatively less sensitive to process variations and pico-watt power consumption and small core area are achieved. However, native transistor which is usually not accurately modeled is required, this may increase the design difficulty. For both \(V_{TH}\) and \(\Delta V_{TH}\)-based reference circuits, their output voltage relies on less fundamental parameters (for example, \(V_{TH}\) and \(\mu\) etc.), relatively worse TC performance is expected [28].

Multiple reference voltage and/or current are usually required for large system designs. Unlike current-mode BGRs, CMOS-only reference circuits (including both bandgap and non-bandgap types) usually generate single reference voltage. Additional components (for example buffers, resistors and voltage dividers etc.), area and power consumption are required in order to do this.

V. Conclusion

A new sub-\(\mu\)W current-mode BGR has been presented. It has an inherent curvature-compensation property, together with the lowest theoretical minimum current consumption among published current-mode BGRs. A proof-of-concept prototype has been successfully implemented in a TSMC 90 nm CMOS process and shows competitive results, especially in terms of TC and power consumption. The measured TC without trimming is as low as 10.1 \(\text{ppm/}°\text{C}\) over a temperature range of 70 \(^°\text{C}\), which is lower than the theoretical minimum TC of first-order BGRs and proves the proposed curvature-compensation technique. The average TC over an extended temperature range of

is not fully characterized. Instead, the start-up time is simulated with a 5 pF loading added and found to be 78 \(\mu\)s. Both PSRR and noise performance can be improved by adding decoupling capacitors with a trade-off of slower start-up.

C. Discussion

Table II shows a comparison between the designed BGR and other published state-of-the-art reference circuits. The area of the designed BGR is one of the smallest. It may not be a fair comparison since other designs may be using older CMOS technologies, however it proves the designed BGR takes advantages from the continuing development of CMOS technology and the possibility of implementing high-performance, low-power and small-area BGRs in modern nm CMOS processes. The relatively large line sensitivity is expected as a result of the lower transistor output resistance in nm CMOS processes as aforementioned. Both TC and coefficient of variation could be improved by trimming the resistor ratios [2], [6] with a trade-off of higher testing cost.

Compared to other sub-\(\mu\)W BGRs, the proposed BGR has the best TC performance. Although the BGRs in [14] and [16] are small-size and low-power because of their resistor-less feature, they require relatively large number of transistors which may degrade the noise performance and cause a longer start-up time (6 ms is reported in [14]). The BGR in [15] uses NPN BJTs which is not preferred as the reasons mentioned in Section II-B.

Fig. 12. Measured characteristics of \(V_{TH}\) versus supply voltage.
100 °C is measured to be 53.1 ppm/°C which is competitive to other published sub-μW BGRs.

The measured average power consumption at room temperature is 576 nW, with a small core area of 0.028 mm². The mean of the measured output voltage at 30 °C is 723 mV with a coefficient of variation of 1.3%, which is good enough for many applications without trimming. Implementations of high-precision, low-power and small-area BGRs in state-of-the-art CMOS technology are proved to be possible. To the best of the authors’ knowledge, the designed BGR is the only sub-μW curvature-compensated BGR that can be found in literature.

CMOS-only reference circuits may provide lower power consumption. Nevertheless, design trade-offs such as sensitivity to process variations, precision and flexibility etc. have to be considered as discussed. Thus, it remains an open question whether resistor-based BGRs or CMOS-only reference circuits will deliver ultimate performance, especially in modern nm CMOS processes.

**APPENDIX I**

The theoretical minimum TC of the conventional BGR \( \left( T_{C_{\text{min,convo}}} \right) \), which is shown in Fig. 1, over a certain temperature range (from \( T_L \) to \( T_H \)) is analyzed as follows. Consider only the first- and second-order TCs of \( V_{EB1} \) and assume all other higher-order effects are ignorable, \( V_{EB1} \) can be expressed as

\[
V_{EB1} = V_{BG}(T_R) + a_1 T + a_2 T^2
\]

where \( a_1 \) and \( a_2 \) are the first- and second-order TCs respectively. Hence \( V_O \) is given as

\[
V_O = V_{BG}(T_R) + n \ln(N) \frac{R_2}{R_1} \cdot V_I
\]

Because the conventional topology is first-order temperature-compensated, \( V_O \) becomes

\[
V_O = V_{BG}(T_R) + a_2 T^2
\]

The best BGR TC can be obtained when \( T_R \) is set to the middle of the targeted temperature range, in other words \( T_R = T_L + (\Delta T/2) \), where \( \Delta T = T_H - T_L \). Then we can write \( T_{C_{\text{min,convo}}} \) as

\[
T_{C_{\text{min,convo}}} = \frac{|\Delta V_{I_{\text{min}}}|}{(\Delta T) V_{BG}(T_R)} = \frac{|a_2| (\Delta T/2)^2}{(\Delta T) V_{BG}(T_R)}
\]

From Fig. 7, it can be observed that \( a_2 \approx -1 \mu V/°C^2 \) when \( T \geq 0 °C \). As a result, for the CMOS process used in this work, \( T_{C_{\text{min,convo}}} \) over temperature ranges of 70 °C and 100 °C are approximately 15.1 ppm/°C and 21 ppm/°C respectively. Similar analysis can be applied to other first-order BGRs and same results can be obtained.

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**REFERENCES**


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