A Novel 3-D Vertical FG NAND Flash Memory Cell Arrays Using the Separated Sidewall Control Gate (S-SCG) for Highly Reliable MLC Operation

Moon-Sik Seo, *Bong-Hoon Lee, *Sung-kye Park and Tetsuo Endoh
Center for Interdisciplinary Research, Tohoku University; 6-3 Aramaki-aza-Aoba, Aoba-ku, Sendai, Miyagi, 980-8578, Japan
*Memory R&D Division, Hynix Semiconductor Inc.; San 136-1 Ami-ri, Bubal-eub, Icheon-si, Kyonggi-do, 467-701, Korea
Center Phone: +81-22-795-5260; Fax: +81-22-795-7810; E-mail: endoh@riec.tohoku.ac.jp

Abstract— We propose a novel 3-dimensional (3-D) vertical floating gate (FG) type NAND flash memory cell arrays using the Separated - Sidewall Control Gate (S-SCG). This novel cell consists of one cylindrical FG with a line type control gate (CG) and S-SCG structure. For simplifying the process flow, we realized the common S-SCG lines by using the pre-stacked poly silicon layer, through which variable medium voltages are applied not only to control the electrically inverted S/D region but also to assist the program and erase operation.

We successfully demonstrate the normal flash cell operation and show its superior performances in comparison with the conventional 3-D NAND cells by using the cylindrical 3-D device simulation. It is shown that the proposed cell can realize the highest CG coupling ratio, low voltage cell operation of program with 15V at Vth=4V and erase with 7V at Vth=-2V and good on/off read current margin by an order of over 1.5. Moreover, the proposed S-SCG cell array can fully suppress both the interference effects and the disturbance problems at the same time by removing the direct coupling effect in the same cell string, which are the most critical problems of the recent 3-D vertical stacked cell structures. Above all, the proposed cell array has good potential for Terabit 3-D vertical NAND flash cell array with highly reliable multi level cell (MLC) operation.

Keywords- 3-D Vertical Stackde Cell, Cylindrical FG, GAA, NAND flash memory, Floating Gate, Sidewall Control Gate, S-SCG

I. INTRODUCTION

The market of NAND flash memory is becoming larger and larger for computers and battery-powered systems, and its applications have expanded from highly reliable solid-state device (SSD) for high-end servers to low cost USB for data storage. However, the scaling to sub 1Xnm technology is becoming difficult due to some physical limitations, such as the interference effects, the disturbance problems and the quantity of stored charge.

In order to overcome these scaling issues and to reduce the bit cost, the floating gate (FG) type 3-dimensional (3-D) vertical stacked surrounding gate (S-SGT) cell array [1] has been proposed in 2001. Recently, the charge trap (CT) type 3-D vertical stacked cell arrays, such as BiCS [2][3][4], P-BiCS [5] and TCAT [6], have been researched to reduce the bit cost of NAND flash memory. Furthermore, in order to overcome the reliability issues of the CT type SONOS and TANOS cells, new 3-D vertical FG type flash cell arrays, such as ESCG [7] and DC-SF [8], have been proposed. However, critical issues are still present in the recent 3-D vertical NAND technologies.

Most important of all is the multi level cell (MLC) operation scheme, which have reduced the bit cost of NAND flash memory. In order to realize the MLC operation, the reliability characteristics and the distribution of the programmed Vth are key factors. In these points of view, the CT type NAND cell has some disadvantages due to its inherently poor reliability characteristic, and its charge spreading issues along the charge trap layer. In addition, the distribution of programmed Vth is mainly affected by the interference and disturbance effects, and the direct coupling effects from neighboring cells of the same string are the most critical issues of recent 3-D vertical NAND cell arrays, instead of the indirect coupling effect, which was critical in conventional planar type NAND cell arrays.

Another concern for the 3-D vertical stacked NAND cell array is the scaling limitation by high voltage cell operation, which limit the scaling beyond sub 1X-nm technology due to the dielectric thickness of about 20nm. Therefore, the bit cost of 3-D vertical stacked NAND cell array is directly proportional to the number of cell stacks, and the process complexity is the most critical factor to stack cells.

In this paper, in order to overcome these issues of conventional 3-D vertical NAND cell arrays, we propose the 3-D vertical FG type NAND flash memory cell array with Separated - Sidewall Control Gate (S-SCG) technique for highly reliable MLC operation; and we successfully demonstrate its superior performance with high speed program/erase operation, good read current margin, and fully suppressed interference and disturbance effects.

II. CONCEPT OF THE PROPOSED S-SCG NAND

Recently, 3-D vertical FG type NAND cell arrays have been proposed to overcome the reliability issues of the CT type 3-D vertical NAND cell arrays. Figure 1 shows the birds eye view of the recent 3-D vertical FG type NAND cell structure of (a) ESCG and (b) DC-SF. With the SCG structure, the S/D region can be implemented by electrically inverting the pillar surface, and high CG coupling capacitance can also be achieved simultaneously. However, there are issues of interference and disturbance problems resulting from the direct coupling effect from neighboring cells of the same string.

To overcome the issues of recent 3-D vertical NAND, we propose a novel 3-D vertical FG type NAND cell arrays using the S-SCG. Figure 2 shows (a) the birds eye view of unit cell of S-SCG, (b) cross sectional views and (c) equivalent circuit of the 3 bit cell arrays by using the S-SCG. Its horizontal feature
size is about $24F^2 (=6F*4F)$ with 2X-nm technology and the vertical height of 2F can be achieved by using pre-stacked SCG.

The operation conditions of the proposed S-SCG NAND cell array are also fully reviewed in Table I. By using the proposed S-SCG cell arrays, the same operation condition as the conventional planar FG NAND can be achieved; especially, the bulk erase is successfully realized by using the electrically inverted S/D technique as shown in Figure 3. Also, to prevent the recent direct interference and disturbance problems, we control the voltage levels to the SCG regions to 8V in program, 0V in erase and 3.5V in read operation.

One example of the process sequence is briefly displayed in Figure 4. The sequential process is as follows: (1) 3-different layers including poly-silicon layers for the SCG are sequentially deposited, (2) and (3), pillar and FG regions are cylindrically etched, (4) cylindrical FG region is deposited by using the unidirectional etching process, (5) and (6), tunnel oxide and poly silicon pillar are deposited, and finally (7) and (8), the CG is self aligned by using the etching ratio and silicid process. The most notable process is the self-aligned process using the difference of the etching ratio among the 3-departed layer, and the data-line select gate (DSG) and sourceline select gate (SSG) are also formed simultaneously with the CG (or SCG) as shown in Fig. 2 (b).

### III. RESULTS AND DISCUSSION

In order to evaluate the characteristics of the proposed S-SCG cell in comparison with the conventional 3-D FG type cell, we performed 3-D cylindrical TCAD simulations in the vertical direction. Figure 5 show (a) the concept of the cylindrical coordination and (b) unit cell structures of the 3-D FG NAND cell. We realize the 8-cells NAND string to implement the unselected cell effect, and decreased the mobility to reflect the mobility degradation effect by the trap density in the pillar region.

First of all, we show the elements of FG coupling capacitance of 30nm design rules in Figure 6. The proposed S-SCG cell achieves the highest CG coupling ratio, which is constructed by both FG-CG and FG-SCG capacitance. Figure 7 shows the Vth dependency on the amount of FG charge (Qfg), and furthermore shows that the proposed S-SCG cell has the most abrupt slope. This is possible due to the low FG-CG coupling capacitance in read operation by applying a low voltage of 3.5V in the SCG region. This is one of the merits for MLC operation because we can enlarge the program Vth with the same Qfg. On the other hand, the ESCG and DC-SF cells have a slight Vth dependence with Qfg due to the high CG coupling capacitance in read operations; especially, the Vth dependence in erase status is very serious due to the parasitic transistor effect of the SCG region.

The Vth when the CG is applied with the program and erase operation voltage are shown in Figure 8 and Figure 9. In the proposed S-SCG cell, the program voltage is dramatically decreased as we increase the SCG voltage (Vscg). On the other hand, as we decrease Vscg, the erase voltage is significantly decreased. As a result, we can achieve a low voltage cell operations during program of 15V at Vth=4V and during Erase of 7V at Vth=2V, by applying a different Vscg bias at program and erase operation of 8V and 0V respectively. Even if we apply only half of the conventional program voltage to SCG node, the proposed S-SCG cell realizes a high-speed program operation due to its excellent coupling ratio as shown in Figure 5.

Among all of the recent 3-D cells, the mobility is mainly degraded by the trap charges of poly silicon grain boundaries in the pillar region, and estimating its read current margin is very difficult. In case of the proposed S-SCG cell, we can sufficiently increase the Iread current by increasing the Vread bias, because it has the smallest FG-NCG coupling capacitance. Figure 10 shows the Iread characteristics with the Vread bias of neighboring CG in the proposed S-SCG cell arrays, and we show that our proposed structure can achieve a sufficient on/off read current margin by over 1.5 orders.

In the 3-D vertical NAND cell, the direct disturbance effects from the high voltages of the passing CG and SCG become more serious due to the high CG coupling ratio as shown in Figure 11 (a) and (b). In the case of the proposed S-SCG cell, we can combine the Vpass (or Vread) and Vscg to prevent direct disturbance effects as shown in Fig11 (c). As a result, we can increase the Vscg to 8V in program operation to improve the program efficiency, and the Vpass to 9V in read operation to reduce the external resistance of neighboring cells.

Sequentially, we confirmed the interference $\Delta$Vth of select gate cell (SGC), as the Vth in neighboring gate cells (NGC) changes from -2V to 4V. In recent junction-less 3-D vertical NAND cells, two critical interference coupling paths exist; one is the indirect and the other is direct coupling path as shown in Figure12 (b). The SCG structure can sufficiently suppress the indirect interference effect; however, the direct coupling from neighboring FG to the channel of SGC remains a very serious problem. Especially, the ESCG and DC-SF cells have remarkable interference problems by this direct coupling effect, which directly influences the parasitic transistor below the SCG. To suppress this direct coupling effect, our proposed S-SCG cell applies the SCG voltage to control the parasitic transistor.

Finally, we show the MLC feasibility and the number of stacked cells in comparison with conventional 3-D cells in Table II. The proposed S-SCG cell fully suppresses both the interference effect and the disturbance problem with good performance, and it has good potentials of highly reliable MLC operation. The vertical cell height is also sufficiently decreased compared to that of the conventional FG cell by using a pre-deposited SCG layer. Figure 13 shows the effective cell size with 3-D vertical NAND cell schemes at 20nm technology. Although the cell size of the proposed S-SCG cell is larger than that of CT type NAND cell by about 60%, we can obtain cheaper effective bit costs by implementing the 2bit MLC operation. Moreover, we can achieve less than half of the effective bit cost by implementing the 3bit MLC (TLC) operation to the proposed S-SCG cell.

### IV. CONCLUSION

In this paper, we proposed a novel 3-D vertical FG NAND flash memory cell arrays using Separated - Sidewall Control Gate (S-SCG). We successfully demonstrated the flash cell operation of this novel cell structure with high-speed program erase operation and sufficient read current margin by using the 3-D cylindrical TCAD simulation. Moreover, we found that the
proposed S-SCG cell array has good potentials of MLC operation by fully suppressing both the interference effect and disturbance characteristics by removing the direct coupling effect in the same cell strings. In conclusion, the 3-D vertical FG NAND cell array using S-SCG can be one of the major candidates for Terabit NAND flash memory with its merits of reducing effective bit costs with highly reliable MLC operation.

ACKNOWLEDGMENT

This work also has been supported in part by a grant from “Research of Innovative Material and Process for Creation of Next-generation Electron Devices” of CREST of Japan Science and Technology Agency (JST). The authors also would like to appreciate S.K. Lee, S.J. Hong and S.W. Park for encouragements on this paper.

REFERENCES


Figure 1. The birds eye views of the recent 3-D vertical FG type NAND cell Scheme; (a) ESCG and (b) DC-SF

Figure 2. A novel 3-D vertical FG NAND with S-SCG; (a) birds eye view and (b) cross sectional view in WL direction and (c) equivalent circuit in Data Line (DL) direction of 3bit cell Array.

TABLE I. OPERATING CONDITIONS OF THE S-SCG CELL ARRAYS

<table>
<thead>
<tr>
<th>Select WL</th>
<th>Program</th>
<th>Inhibit</th>
<th>Read</th>
<th>Erase</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pass WL</td>
<td>Vppass (5V)</td>
<td>Vppass (5V)</td>
<td>Vread (9V)</td>
<td>0V</td>
</tr>
<tr>
<td>SCG</td>
<td>Vccp (3.5V)</td>
<td>Vccp (3.5V)</td>
<td>Vcc (3.5V)</td>
<td>Vcc (3.5V)</td>
</tr>
<tr>
<td>Data Line</td>
<td>0V</td>
<td>Vcc (3.5V)</td>
<td>Vcc (3.5V)</td>
<td>FT</td>
</tr>
<tr>
<td>Source Line</td>
<td>0V</td>
<td>0V</td>
<td>0V</td>
<td>FT</td>
</tr>
<tr>
<td>D/L SG</td>
<td>Vcc (3.5V)</td>
<td>Vcc (3.5V)</td>
<td>Vread (5V)</td>
<td>FT</td>
</tr>
<tr>
<td>S/L SG</td>
<td>0V</td>
<td>0V</td>
<td>Vread (5V)</td>
<td>FT</td>
</tr>
<tr>
<td>Bulk</td>
<td>0V</td>
<td>0V</td>
<td>0V</td>
<td>Verase</td>
</tr>
</tbody>
</table>

Figure 3. The potential distribution of bulk erase operation

Figure 4. One example of the process sequence; The most unique process is the self-aligned process using the difference of the etching ratio among the 3-departed layer

Figure 5. The 3-D cylindrical TCAD simulation; (a) the concept of the cylindrical coordination and (b) unit cell structures of the 3-D FG NAND

Figure 6. The FG coupling capacitance of 3-D vertical FG NAND cells; (a) the elements and (b) cross sectional view of FG coupling capacitances.

Figure 7. The Vth dependency with the amount of the FG charge (Qfg). The proposed S-SCG cell has the most abrupt slope.
Figure 8. The program Vth (a) with Vscg bias in S-SCG cell, (b) with other 3-D vertical FG NAND cells.

Figure 9. The erase Vth by the bulk erase operation; (a) with Vscg bias in S-SCG cell, (b) with other 3-D vertical FG NAND cells.

Figure 10. The Iread margin (a) with Vread bias in S-SCG cell and (b) cross sectional view of read operation.

TABLE II. SUMMARY OF 3-D NAND CELLS
The MLC operation is determined by cell performances, such as reliability characteristics, interference effects and disturbance problems. The number of cell stacks is also affected by the inter poly directric (IPD) thickness, which is unscaleable in high voltage program operations.

<table>
<thead>
<tr>
<th>D/R=20nm Technology (Aspect Ratio=32)</th>
<th>CT type</th>
<th>FG type</th>
</tr>
</thead>
<tbody>
<tr>
<td>BiCS</td>
<td>C-FG</td>
<td>ESCG</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Cell Performances</th>
<th>MLC feasibility</th>
<th>Minimum IPD</th>
<th>Minimum Gate Electrode</th>
<th>Cell height</th>
<th># of stacked cell</th>
</tr>
</thead>
<tbody>
<tr>
<td>C/R</td>
<td>(bit/cell)</td>
<td>(nm)</td>
<td>(nm)</td>
<td>(nm)</td>
<td></td>
</tr>
<tr>
<td>Reliability</td>
<td>Not Easy (1bit)</td>
<td>-</td>
<td>-</td>
<td>40</td>
<td>16</td>
</tr>
<tr>
<td>Disturbance</td>
<td>Normal (2bit)</td>
<td>12</td>
<td>6</td>
<td>60</td>
<td>16</td>
</tr>
<tr>
<td>Interference</td>
<td>Not Easy (1bit)</td>
<td>12</td>
<td>6</td>
<td>50</td>
<td>11</td>
</tr>
<tr>
<td></td>
<td>Easy (3bit)</td>
<td>7</td>
<td>6</td>
<td>40</td>
<td>13</td>
</tr>
</tbody>
</table>

G=Good, NG=Not Good, VG=Very Good

Figure 11. The direct disturbance characteristics; (a) disturbance effect with Vpass and Vscg bias in S-SCG cell, (b) disturbance characteristics with other 3-D vertical FG NAND cells, (c) disturbance free window in S-SCG cell and (d) cross sectional view of direct disturbance coupling path.

Figure 12. The interference characteristics; (a) interference effect in other 3-D vertical FG NAND cells and (b) cross sectional view of interference coupling paths of the conventional ESCG cell array.

Figure 13. The effective cell size of the proposed S-SCG cell in comparison with other 3-D vertical NAND cells at 20nm technology.